REMARKS

The Office Action dated June 23, 2005, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

By this Amendment, claims 1, 4-6, 16 and 21 are amended. Claims 1, 2 and 4-21 are pending in the present application, and are respectfully submitted for reconsideration.

Entry of this Amendment is proper under 37 C.F.R. § 1.116 since this Amendment: (a) places the application in condition for allowance for reasons discussed herein; (b) does not raise any new issue regarding further search and/or consideration since the Amendment amplifies issues previously discussed throughout prosecution; (c) does not present any additional claims without canceling a corresponding number of finally-rejected claims and (d) places the application in better form for appeal, should an appeal be necessary. The Amendment is necessary because it is made in reply to arguments raised in the rejection. Entry of the Amendment is thus respectfully requested.

Claims 1-2, 4-5 and 16-21 Rejected under 35 U.S.C. § 103(a)

Claims 1-2, 4-5 and 16-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takahashi et al. (Japanese Patent No. JP40927070, hereinafter "Takahashi"). This rejection is respectfully traversed.

Claim 1 recites an input circuit comprising, among other features, an inverter circuit connected to a drain of the first transistor, for inverting the node signal and

generating a data strobe signal; and a current regulating circuit, connected to the differential circuit, which increases an amount of the current flowing through the differential circuit in response to the data strobe signal when the first transistor changes its state from an activated state to a deactivated state in response to the external signal and the node signal rises, such that only a rising delay time of the node signal is shortened.

Claim 16 recites an input circuit comprising, among other features, a first inverter having an input terminal connected to a second node between the first and fifth transistors and an output terminal connected to the gate of the fourth transistor, a node signal having a rising edge and a falling edge is generated at the second node in accordance with a current flowing through the first and second transistors and a data strobe signal is generated at the output terminal of the first inverter, and wherein the fourth transistor operates to increase an amount of the current flowing through the second transistor in response to the data strobe signal when the first MOS transistor changes its state from an activated state to a deactivated state in response to the data signal and the node signal rises, such that only a rising delay time of the node signal is shortened.

Claim 21 recites a semiconductor integrated circuit comprising, among other features, an inverter circuit connected to a drain of the first transistor, for inverting the differential output signal and generating the second data strobe signal; and a current adjustment transistor coupled to the sources of the first and second transistors, a third gate of the current adjustment transistor receiving the data strobe signal of the inverter

circuit, wherein the current adjustment transistor operates to increase an amount of the current flowing through the differential circuit in response to the second data strobe signal when the first transistor changes its state from an activated state to a deactivated state in response to the first data strobe signal and the differential output signal rises, such that a rising delay time of the differential output signal is shortened.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicant's invention.

In making the rejection, the Office Action acknowledges that Takahashi "does not disclose the limitation that the regulating circuit current increases an amount of the current flowing through the differential circuit to be increased in response to the node signal when the first transistor changes its state from an activated state in response to an external signal and the node signal rises, such that only rising delay time of the node signal is shortened." See, page 2 of Office Action. Furthermore, the Office Action noted that "selecting an optimum number of feedback delay elements of Takahashi et al, i.e., one inverter, for providing a predetermined speed cycle time required by a predetermined system in which the circuit of Takahashi et al is to be used is considered to be a matter of a design expedient for an engineer." See, page 3 of Office Action.

Applicant respectfully disagrees with the Office Action's position, and therefore respectfully traverses.

It is submitted that in one embodiment of the present invention, the present invention uses one inverter and the current regulating circuit (for example, the fourth

transistor of claim 16, current adjustment transistor of claim 21) with the intention to shorten the rising delay time of a node signal (differential output signal, for example).

In contrast, Takahashi merely uses one inverter V6, the inverter group DL2, and the transistor N6 with the intention to shorten the falling delay time of a next node signal n4 after a node n4 signal rises as shown in Figs. 4 and 5. Accordingly, the inverter group DL2 of Takahashi elongates a cycle speed of an amplifier because Takahashi turns off the transistor N3 to completely rise a node signal n4 to a high level, and then turns on the transistor N6 after the delay time of the inverter group DL2 has elapsed to lower the voltage of the node signal n4 from the high level by ΔV. Therefore, Takahashi fails to achieve the high-speed operation, and it is submitted that one skilled in the art would not have a motivation to employ Takahashi for the purpose of shortening the rising time of a node signal.

Furthermore, Applicant submits that Takahashi fails to disclose providing a data strobe signal generated by the inverter to the current regulating circuit. Rather, Takahashi merely provides an internal signal generated by the inverter V6 and the inverter group DL2.

Hence, Applicant submits that the features disclosed in Takahashi are neither comparable nor analogous to the limitations recited in the claims of the present application, and therefore Takahashi fails to disclose each and every element recited in claims 1, 16 and 21 of the present application.

In order to establish a *prima facie* case of obviousness, each feature of a rejected claim must be taught or suggested by the applied art of record. See M.P.E.P.

§2143.03 and *In re Royka*, 490 F.2d 981 (CCPA 1974). As explained above, Takahashi fails to teach or suggest each and every feature recited in claims 1, 16 and 21. Accordingly, for the above provided reasons, Applicant respectfully submits that claims 1, 16 and 21 are not rendered obvious under 35 U.S.C. § 103 by Takahashi, and are allowable.

As claims 2, 4, 5 depend from claim 1, and claims 17-20 depend from claim 16, Applicant submits that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Applicant respectfully requests withdrawal of the rejection.

Claims 6-20 Rejected Under 35 U.S.C. § 103(a)

Claims 6-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Figure 1 of Applicant's admitted prior art ("AAPA") in view of Takahashi. Applicant respectfully traverse the rejection.

Claim 6 recites a semiconductor integrated circuit comprising, among other things, an inverter circuit connected to a drain of the first transistor, for inverting the node signal and generating a data strobe signal, and a current regulating circuit, connected to the differential circuit, which increases an amount of the current flowing through the differential circuit in response to the data strobe signal when the first transistor changes its state from an activated state to a deactivated state in response to the external signal and the node signal rises, such that only a rising delay time of the node signal is shortened.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicant's invention.

In making the rejection, the Office Action affirms that AAPA "does not discloses [sic] that the amplifiers have a current regulating circuit increases an amount of the current flowing through the differential circuit in response to the node signal such that only rising delay time of the node signal is shortened." The Office Action relies on Takahashi and states that "Takahashi et al teaches a modified amplifier circuit ..."

Applicant respectfully disagrees with the Office Action's position, and therefore traverses for at least the reasons stated above. In particular, it is submitted that the cited prior art fails to disclose or suggest at least the limitations of "an inverter circuit connected to a drain of the first transistor, for inverting the node signal and generating a data strobe signal, and a current regulating circuit, connected to the differential circuit, which increases an amount of the current flowing through the differential circuit in response to the data strobe signal when the first transistor changes its state from an activated state to a deactivated state in response to the external signal and the node signal rises, such that only a rising delay time of the node signal is shortened," with respect to claim 6; and the limitations of "a first inverter having an input terminal connected to a second node between the first and fifth transistors and an output terminal connected to the gate of the fourth transistor, a node signal having a rising edge and a falling edge is generated at the second node in accordance with a current flowing through the first and second transistors and a data strobe signal is generated at the output terminal of the first inverter, and wherein the fourth transistor operates to

increase an amount of the current flowing through the second transistor in response to the data strobe signal when the first MOS transistor changes its state from an activated state to a deactivated state in response to the data signal and the node signal rises, such that only a rising delay time of the node signal is shortened," with respect to claim 16, and therefore are allowable.

As claims 7-15 depend from claim 6, and claims 17-20 depend from claim 16, Applicant submits that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Applicant respectfully requests withdrawal of the rejection.

Conclusion

In view of the above, Applicant respectfully submits that each of claims 1-2 and 4-21 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-2 and 4-21 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time.

Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, referring to client-matter number 108075-09014.

Respectfully submitted,

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Enclosure: Petition for Extension of Time (one month)